REMARKS

Claims 1-32 are pending in the present application. Claims 1-3, 5-16, and 18-32 stand rejected; and claims 4 and 17 stand objected to. By this Amendment, claims 4 and 17 have been amended. This application continues to include claims 1-31.

The Examiner has objected to claims 4 and 17 as being dependent upon a rejected base claim, but has indicated that claims 4 and 17 contain allowable subject matter, and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the indication of allowability regarding claims 4 and 17.

Applicants have so amended claims 4 and 17, and accordingly believe claims 4 and 17 to be in condition for allowance.

Accordingly, Applicants respectfully request that the objection to claims 4 and 17 be withdrawn.

Claims 1-5, 10, 11, 16-19, and 28-32 have been provisionally rejected under the judicially created doctrine of double patenting as being unpatentable over claims 1-5, 9, 10, 14-17, and 27-31, respectively, of copending Application No. 09/895782.

Submitted herewith is a Terminal Disclaimer disclaiming the terminal part of any patent granted on the present application which would extend beyond the expiration date of the full statutory term of any patent granted on copending Application No. 09/895782.

Accordingly, Applicants respectfully request that the provisional rejection of claims 1-5, 10, 11, 16-19, and 28-32 under the judicially created doctrine of double patenting be withdrawn.

Claims 1-3, 5-16, 18, 19, and 22-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan, U.S. Patent No. 6,359,946 B1. Applicants respectfully request reconsideration of the rejection of claims 1-3, 5-16, 18, 19, and 22-32 in view of the following.

Applicants hereby incorporate by reference their arguments as set forth in their previous Response, mailed 9/8/2005.

Ryan is directed to synchronization, i.e., synchronizing to asynchronous data transmissions (col. 1, lines 5-9). Ryan discloses an asynchronous data signal 10 that may be a serial digital data stream having a bit-rate period 12, which corresponds inversely to the frequency at which data is communicated by asynchronous data signal 10 (col. 7, lines 13-16). Ryan also discloses as follows:

> A counter 20 is provided to count the time between sample edges of the sample clock 16 and data transitions of the asynchronous data signal 10. Counter 20 is clocked by a high speed clock that has a frequency at least twice as fast as the bit rate of data signal 10. Counter 20 receives signals indicative of when a transition, or edge, occurs on asynchronous data signal 10 and when a sample edge of sample clock 16 occurs, as indicated at reference numeral 22. Control input 22 restarts the counter whenever one of these events occurs. Thus counter 20 may be thought of as a stop watch that measures the time between consecutive occurrences of a transition in data signal 10 or sample clock 16. Counter 20 outputs a count value measuring the time between a sample clock edge and a data signal transition edge to comparitor 26. Comparitor 26 compares this count value to a dead-band value 24. Dead-band value 24 is a predetermined value indicating the minimum time between a transition on data signal 10 and a sample edge of sample clock 16 for a valid sample to occur. Comparitor 26 checks whether or not this minimum spacing or dead-band value 24 is violated. (col. 7, line 50 to col. 8, line 3). (Emphasis added).

Ryan further discloses, with reference to Fig. 5, a clock synchronizer for synchronizing a sample clock 16 to an asynchronous data signal 10 and for detecting when a sample clock 16 transition occurs too close to a data transition on data signal 10 (col. 9, lines 21-24). A bit-rate counter 60 provides a count clock signal 78 having a frequency approximately equal to the bit rate

of the asynchronous data signal 10, and may be clocked by a high speed clock that is at least twice the frequency of the data bit rate of data signal 10 and preferably at a much higher frequency than data signal 10 (col. 9, lines 24-30).

Clock signal 78 may be a single pulse such as provided by the terminal count signal of a counter indicating when the counter has reached the count indicated by bit-rate value 72 or has counted down to zero from the bit-rate value 72 (col. 9, lines 33-38).

A phase counter 70 is provided to generate sample clock 16. Phase counter 70 may be programmed with a phase delay value 82 such that phase counter 70 generates SCLK 16 at the same frequency as clock signal 78 from bit-rate counter 60, but delayed by a phase delay as specified by phase delay value 82 (col. 9, lines 48-53).

SCLK 16 may be synchronized to data signal 10 so that transitions of SCLK 16 will indicate times at which data signal 10 is valid, by employing a subtracter 62 to subtract the current count 76 as provided by bit-rate counter 60 from bit-rate value 72, which functions to provide a measurement of the difference between bit-rate value 72 and the current count value 76 of bit-rate counter 60 (col. 9, line 66 to col. 10, line 5). The output of subtracter 62 is received by comparitor 64 which functions to compare whether or not the difference as determined by subtracter 62 is less than dead-band value 24 (col. 10, lines 5-8).

Edge detector 66 is provided to detect data transitions on data signal 10 by providing an edge signal 46, which is indicative of when a data transition has occurred on data signal 10 (col. 10, lines 8-12).

Applicants believe that claims 1-3, 5-16, 18, 19, and 22-32 patentably define Applicants' invention over Ryan for at least the reasons set forth below.

Claim 1 is directed to a method for effecting synchronous pulse generation for use in variable speed serial communications. Claim 1 recites, in part, generating a difference signal representing a signal level difference between at least two data stream signals. Claim 1 also recites, in part, if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated.

As set forth in Applicants' previous response, Ryan does not disclose, teach, or suggest generating a difference signal representing a signal level difference between at least two data stream signals, as recited in claim 1.

The Examiner acknowledges that Ryan is silent as to generating a difference signal.

However, in the Response to Arguments, the Examiner asserts that generating a difference signal is interpreted by the Examiner as reception of a differential signal and converting it to a single ended signal, relying on an IEEE definition.

Without regard to the Examiner's asserted interpretation, as acknowledged by the Examiner, Ryan simply does not disclose, teach, or suggest generating a difference signal representing a signal level difference between at least two data stream signals.

Ryan also does not disclose, teach, or suggest reception of a differential signal and converting it to a single ended signal.

Rather than at least two data stream signals, Ryan only discloses a single data signal 10, which does not disclose, teach, or suggest a difference signal representing a signal level difference between at least two data stream signals.

MPEP 2143 provides that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (Emphasis added).

However, as acknowledged by the Examiner, Ryan is silent as to generating a difference signal, as recited in claim 1, and accordingly, Ryan does not disclose, teach, or suggest generating a difference signal representing a signal level difference between at least two data stream signals.

Since Ryan does not disclose, teach, or suggest generating a difference signal representing a signal level difference between at least two data stream signals, as recited in claim 1, a prima facie case of obviousness has not been established as against claim 1.

In addition, the Examiner has not demonstrated the effective dates of the definitions relied upon by the Examiner in the Response To Arguments, including the definition obtained via IEEE 100.

Since the relied-upon definition was not shown by the Examiner to have an effective date or to have been in use at the time Applicants' invention was made, such definition may not be used as part of the rejection of Applicants' claims under 35 USC §103(a), and may not be employed in interpreting Applicants' claims.

Ryan also does not disclose, teach, or suggest determining whether a signal level of said difference signal has changed, as set forth in Applicants' previous Response.

The Examiner asserts, in the Response to Arguments, that Ryan discloses detecting a signal edge change for an incoming data signal, based on Ryan reference number 66, and declines

to withdraw the rejection, asserting that Applicants' argument regarding the difference signal as a design choice is unfounded.

However, the Ryan reference number 66 is an edge detector for providing an edge signal 64, and simply does not disclose, teach, or suggest determining whether a signal level of a difference signal has changed.

A finding of obvious design choice is precluded where the claimed structure and the function it performs are different from the prior art. *In re Gal*, 980 F.2d 717, 25 USPQ2d 1076 (Fed. Cir. 1992); *In re Chu*, USPQ2d 1089 (Fed. Cir. 1995). (Emphasis added).

However, the claimed structure and function performed in accordance with claim 1 are clearly different from Ryan, since the Ryan edge detector 66 operates on the single incoming data signal 10 to detect a signal edge and provide edge signal 64, whereas Applicants' difference signal represents a signal level difference between at least two data stream signals, as recited in claim 1.

Accordingly, the claimed structure and function performed in accordance with claim 1 are clearly different from Ryan art, and hence, a finding of obvious design choice is precluded.

In addition, claim 1 recites, in part, if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed.

However, Ryan simply does not disclose, teach, or suggest a decision step wherein if a current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed.

Rather, the Ryan edge detector 66 operates on data signal 10, without regard to a current count value corresponding or not corresponding to a sample count value, and without the IF-THEN logic recited in claim 1.

Claim 1 also recites, in part, if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated.

Ryan simply does not disclose, teach, or suggest ignoring further changes in the signal level of a difference signal, as recited in claim 1, much less the IF-THEN-UNTIL logic recited in claim 1.

In the Response To Arguments, the Examiner asserts that the immediately preceding limitation of claim 1 does not affect the operation of the other steps of the claim.

However, without regard to the Examiner's assertion, the claim 1 limitation, "if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated," is a limitation that simply is neither disclosed, taught or suggested by Ryan.

MPEP 2143 provides that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (Emphasis added).

Since Ryan does not disclose, teach, or suggest if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated, as recited in claim 1, a prima facie case of obviousness has not been established as against claim 1.

In addition, the IF-THEN and IF-THEN-UNTIL logic recited in claim 1, i.e., if said signal level of said difference signal has changed then performing a step of ignoring further changes in

said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated, clearly effects and controls the output of Applicants' claimed method for effecting synchronous pulse generation for use in serial communications, as recited in claim 1.

Accordingly, for at least the reasons set forth above, Applicants respectfully submit that Ryan does not disclose, teach, or suggest the subject matter of claim 1. Claim 1 is thus believed allowable in its present form.

Claims 2, 3, and 5-9 depend, directly or indirectly, from claim 1. Accordingly, claims 2, 3, and 5-9 are believed to be in condition for allowance in view of their dependence from claim 1, for at least the reasons set forth above with respect to claim 1. In addition, claims 2, 3, and 5-9 further and patentably define the present invention over Ryan.

For example, claim 5 is directed to the method of claim 1, wherein said step of ignoring further changes in said signal level of said difference signal further comprises the steps of: resetting said counter; determining whether said current count value corresponds to said sample count value; and if said current count value does not correspond to said sample count value then performing a step of incrementing said counter each cycle of said clock signal until said current count value corresponds to said sample count value at which time a step of sampling said difference signal to extract data from said difference signal is performed.

As set forth above with respect to claim 1, Ryan does not disclose, teach, or suggest the step of ignoring further changes in the signal level, as recited in claim 5.

MPEP 2143 provides that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (Emphasis added).

Since Ryan does not disclose, teach, or suggest all the limitations of claim 5, a prima facie case of obviousness has not been established as against claim 5.

Claim 5 is thus believed allowable in its own right.

Claim 6 is directed to the method of claim 1, wherein a communication link with which said communication link speed is associated is an IEEE-1394b bus.

Ryan simply does not disclose, teach, or suggest wherein a communication link with which said communication link speed is associated is an IEEE-1394b bus, as recited in claim 6, and as acknowledged by the Examiner.

However, in the Response To Arguments, the Examiner cites IEEE 1394b, "which could be easily applied to a generic communications adapter, and would be obvious to one of ordinary skill in the art at the time of the invention."

Although the Examiner asserts that it would be obvious to apply IEEE-1394b to Ryan, MPEP 2143.01(III) and (IV) provide that the fact that the claimed invention can be modified or is within the capabilities of one or ordinary skill in the art is not sufficient by itself to establish prima facie obviousness, and that without a motivation to modify or combine, a rejection based on a prima facie case of obviousness is improper.

In addition, MPEP 2142 provides that the initial burden for a prima facie case of obviousness is on the Examiner to provide some suggestion of the desirability of doing what the inventor has done. However, the Examiner has neither provided a motivation to modify or combine, or some suggestion of the desirability of doing what Applicants' have done.

Accordingly, it would not be obvious to modify Ryan, as asserted by the Examiner, to achieve Applicants' inventions of claim 6.

Claim 10 is directed to a method of extracting data from a difference signal representing a signal level difference between two data stream signals. Claim 10 recites, in part, if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of sampling said difference signal to extract data from said difference signal is repeated.

Claim 10 is believed allowable for substantially the same reasons as set forth above with respect to claim 1.

Claims 11-18 depend, directly or indirectly, from claim 10. Accordingly, claims 11-18 are believed to be in condition for allowance in view of their dependence from claim 10.

In addition, claims 11-18 further and patentably define the present invention over the cited references. For example, claim 12 is believed to be in condition for allowance for substantially the same reasons set forth above with respect to claim 6. Claim 18 is believed to be in condition for allowance for substantially the same reasons set forth above with respect to claim 5.

Claim 19 is directed to a variable speed communications device. Claim 19 recites, in part, a receiver having a first input, a second input and a first output, said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data signal stream, wherein said receiver processes said first data signal stream and said second data signal stream to generate a difference signal representing a difference between said first data signal stream and said second data signal stream.

Ryan simply does not disclose, teach, or suggest a first data stream and a second data stream,

as recited in claim 19.

In addition, for substantially the same reasons as set forth above with respect to claim 1, Ryan does not disclose, teach, or suggest generating a difference signal representing a difference between the first data signal stream and the second data signal stream, as recited in claim 17. As acknowledged by the Examiner, Ryan is silent with respect to a "difference signal."

Also, any receiver of Ryan Fig. 5 does not disclose, teach, or suggest the first input being adapted for receiving a first data signal stream and the second input being adapted for receiving a second data signal stream, as recited in claim 19, from which the difference signal is generated.

Accordingly, Ryan does not disclose, teach, or suggest all the limitations of claim 19, and hence, a prima facie case of obviousness has not been established as against claim 19, as required by MPEP 2143.

Accordingly, for at least the reasons set forth above, Applicants respectfully submit that Ryan does not disclose, teach, or suggest the subject matter of claim 19. Claim 19 is thus believed allowable in its present form.

Claims 22 and 23 depend, directly or indirectly, from claim 19. Accordingly, claims 22 and 23 are believed to be patentable in view of their dependence from claim 19.

Claim 24 is directed to an IEEE 1394b communications device. Claim 24 recites a receiver having a first input, a second input and a first output, said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data stream, wherein said receiver processes said first data signal stream and said second data signal stream to generate a difference signal representing a difference between said first data signal stream and said second data signal stream.

As set forth above with respect to claim 1, rather than at least two data stream signals, Ryan only discloses a single data signal 10.

In addition for substantially the same reasons as set forth above with respect to claim 1, Ryan does not disclose, teach, or suggest generating a difference signal representing a difference between said first data signal stream and said second data signal stream.

Also, the Examiner acknowledges that Ryan is silent as to generating a difference signal, as recited in claim 1.

However, the Examiner asserts, in the Response to Arguments, that generating a difference signal representing a difference between the first data signal stream and the second data signal stream, as recited in claim 24, does not appear to be a novel concept.

MPEP 2143 provides that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (Emphasis added).

Since Ryan does not disclose, teach, or suggest generating a difference signal representing a difference between the first data signal stream and the second data signal stream, as recited in claim 24, then Ryan does not disclose, teach, or suggest all the limitations of claim 24, and hence, prima facie obviousness has not been established.

Claim 24 also recites a synchronous pulse generator having a first clock input, a first difference signal input, a speed input and a synchronous pulse output, said first clock input being adapted for receiving a clock signal, said speed input being adapted to receive a communication speed and said first difference signal input being coupled to said output for receiving said difference signal, wherein said synchronous pulse generator processes said clock signal and said difference signal to generate a synchronous pulse used for extracting data from said difference signal; a serial/parallel translator having a second clock input, a second difference signal input, a synchronous pulse input

and an encoded data output, said second clock input being coupled to said first clock input for receiving said clock signal, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, wherein said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse to generate encoded data for output on said encoded data output; an 8B/10B decoder having a third clock input, an encoded data input and a scrambled data output, said third clock input being coupled to said first clock input for receiving said clock signal, said encoded data input being coupled to said encoded data output for receiving said encoded data, wherein said 8B/10B decoder processes said clock signal and said encoded data to generate scrambled data for output on said scrambled data output; and a descrambler having a fourth clock input, a scrambled data input and a parallel data output, said fourth clock input being coupled to said first clock input for receiving said clock signal, said scrambled data input being coupled to said scrambled data output for receiving said scrambled data, wherein said descrambler processes said clock signal and said scrambled data to generate parallel data for output on said parallel data output.

Ryan simply does not disclose, teach, or suggest a synchronous pulse generator having a first clock input being adapted for receiving a clock signal, a serial/parallel translator having a *second clock input* being *coupled to said first clock input* for receiving said clock signal, an 8B/10B decoder having a *third clock input being coupled to said first clock input* for receiving said clock signal; and a descrambler having a *fourth clock input being coupled to said first clock input* for receiving said clock signal, as recited in claim 24, much less all of the above-recited limitations of claim 24.

In addition, Ryan does not disclose, teach, or suggest any four (4) components that have clock inputs for receiving a clock signal from a first clock input.

Rather, in rejecting claim 24, the Examiner relies extensively on Ryan at column 9, lines 27-33, and on Ryan Figs. 5 and 7, and column 13, lines 23-39. However, the relied-upon Ryan passages are unrelated to and do not disclose, teach, or suggest all of the limitations of claim 24.

Since Ryan does not disclose, teach, or suggest all the limitations of claim 24, prima facie obviousness has not been established, as required by MPEP 2143.

In the Response To Arguments, the Examiner asserts that IEEE 1394b Figs. 4-1 and 10-2 disclose the elements of claim 24. However, IEEE 1394b was not cited as a reference in rejecting claim 24. In addition, IEEE 1394b Figs. 4-1 and 10-2 are generalized figures that simply do not disclose, teach, or suggest all of the above-recited limitations of claim 24.

Further, as set forth above in Applicants previous Response, in contrast to claim 24, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112, or elements 110, 96, 90, to generate encoded data.

In the Response to Arguments, the Examiner asserts that "given that claim requires use of a decoder the output of encoded data is required for decoder to operable and therefore inherent."

However, without regard to the Examiner's assertion, Ryan simply does not disclose, teach, or suggest using out signal 112, or elements 110, 96, 90, to generate encoded data, and hence, does not disclose, teach, or suggest all of the limitations of claim 24.

Accordingly, for at least the reasons set forth above, Ryan does not disclose, teach, or suggest the subject matter of claim 24. Claim 24 is thus believed allowable in its present form.

Claims 25-27 depend, directly or indirectly, from claim 24. Accordingly, claims 25-27 are believed to be in condition for allowance in view of their dependence from claim 24.

Claim 28 is directed to a method for synchronizing a receiver to data. Claim 28 recites, in part, detecting a change in said data; incrementing said count value if no change in said data is detected.

In contrast to claim 28, Ryan simply does not disclose, teach, or suggest incrementing a count value if no change in the data is detected. Ryan simply does not disclose that the operation of the Ryan counter is based on whether a change in the data is or is not detected.

In rejecting claim 28, the Examiner did not which passages of Ryan assertedly disclose, teach, or suggest incrementing a count value if no change in the data is detected, as recited in claim 28.

Applicants respectfully submit that Ryan does not disclose, teach, or suggest incrementing a count value if no change in the data is detected, as recited in claim 28, and accordingly, respectfully request the Examiner to point out with specificity where Ryan discloses the subject matter of claim 28, or to withdraw the rejection of claim 28.

Otherwise, since Ryan does not disclose, teach, or suggest all the limitations of claim 28, prima facie obviousness has not been established, as required by MPEP 2143.

Accordingly, claim 28 is believed allowable in its present form.

Claim 28 also recites, in part, generating a pulse when said counter reaches said sampling count value; and sampling said data using said single clock signal when said pulse is asserted.

As acknowledged by the Examiner, Ryan is silent as to sampling the data using the single clock signal when the pulse is asserted. However, in the Response To Arguments, the Examiner asserts that Ryan discloses the alignment of sampling clock (SCLK) to a master clock phase, "where it is clear that a higher speed clock is used to control the output of sampling clock," relying on Ryan at column 10, lines 26-42.

The relied-upon Ryan passage simply does not disclose, teach, or suggest sampling the data using the single clock signal when the pulse is asserted, as recited in claim 28. Rather than sampling the data using the single clock signal when the pulse is asserted, the relied-upon passage discloses that SCLK 16 is delayed using a delay value 82 so that transitions of SCLK 16 occur far enough from transitions of data signal 10.

Accordingly, for at least the reasons set forth above, Ryan does not disclose, teach, or suggest the subject matter of claim 28.

Claims 29-32 are believed to be allowable due to their dependence from claim 28.

Accordingly, in view of the above, it is respectfully requested that the Examiner withdraw the rejection of claims 1-3, 5-16, and 18, 19, and 22-32 under 35 U.S.C. § 103(a) as being unpatentable over Ryan.

Claims 20-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE-1394b, Draft 1.11. Applicants respectfully request reconsideration of the rejection of claims 1-3, 5-16, and 18, 19, and 20-32 in view of the following.

Claim 20 is directed to the variable speed communications device of claim 19. Claim 20 recites, in part, a serial/parallel translator having a second difference signal input, a synchronous pulse input and an encoded data output, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, and said serial/parallel translator processing said difference signal and said synchronous pulse to generate encoded data, said encoded data being output on said encoded data output.

Claim 20 is believed allowable due to its dependence on otherwise allowable base claim 19.

In addition, as set forth above with respect to claim 24, Ryan simply does not disclose, teach, or suggest generating encoded data, as recited in claim 20. In contrast, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112 to generate encoded data. In addition, IEEE 1394b does not disclose, teach, or suggest generating encoded data, as recited in claim 20.

Accordingly, the combination of Ryan and IEEE-1394b would not yield Applicants' invention, as recited in claim 20.

Further, in rejecting claim 20, the Examiner relies on IEEE 1394b Fig. 10-2. However, Fig. 10-2 is merely a general diagram pertaining to scrambling and coding functions, and does not disclose, teach, or suggest all of the limitations of claim 20.

MPEP 2143 provides that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (Emphasis added).

Since Ryan does not disclose, teach, or suggest all the limitations of claim 20, prima facie obviousness has not been established.

Accordingly, Ryan and IEEE 1394b, taken alone or in combination, do not disclose, teach, or suggest the subject matter of claim 20. Claim 20 is thus believed allowable in its present form.

Claim 21 is directed to the variable speed communications device of claim 20, further comprising a packet receiver/transmitter having a parallel input, said parallel input being coupled to said parallel output of said descrambler for receiving said parallel data.

Claim 21 is believed allowable due to its dependence on otherwise allowable claim 20, and/or on base claim 19.

Accordingly, in view of the above, it is respectfully requested that the Examiner withdraw the rejection of claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Ryan in view of IEEE 1394b.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the amended claims. The pending claims are therefore in condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

Respectfully submitted,

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